Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.021”**

**.021”**

**S-D**

**S-D**

**G**

**G**

**F99**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GATE**

**Mask Ref: PJ99**

**APPROVED BY: DK DIE SIZE .021” X .021” DATE: 5/11/16**

**MFG: InterFET THICKNESS .008” P/N: 2N5116**

**DG 10.1.2**

#### Rev B, 7/1